

**AMENDMENTS TO THE CLAIMS**

1. – 3. (Canceled)

4. (Currently Amended) A driving circuit of a liquid crystal display device comprising:  
a timing controller outputting a polarity-inverting signal and at least one digital signal;  
a source driver;  
a low color scale driving circuit, wherein the low color scale driving circuit generates at least one analog signal and comprises:  
at least one buffer, receiving the polarity-inverting signal and said at least one digital signal outputted from the timing controller; and  
at least one set of transistors, coupled to an output terminal of the buffer for outputting said analog signal~~The driving circuit of claim 3,~~ wherein said set of transistors comprises a PMOS transistor and a NMOS transistor, a gate of the PMOS transistor and a gate of the NMOS transistor coupled to the output terminal of the buffer, a source of the PMOS transistor coupled to the drain of the NMOS transistor, a drain of the PMOS transistor coupled to a power voltage, a source of the NMOS transistor coupled to a ground voltage, the analog signal outputted through the source of the PMOS transistor and the drain of the NMOS transistor.

5. (Previously Amended) A driving circuit of a liquid crystal display device including a timing controller, a source driver and a low color scale driving circuit, the timing controller outputting a polarity-inverting signal, a first digital signal, a second digital signal, a third digital signal and a fourth digital signal, the low color scale driving circuit generating a first analog signal, a second analog signal, a third analog signal and a fourth analog signal and comprising:

a plurality of buffers, receiving the polarity-inverting signal, the first digital signal, the second digital signal, the third digital signal and the fourth digital signal; and

a plurality of sets of transistors which comprise a first set of transistors, a second set of transistors, a third set of transistors, and a fourth set of transistors, respectively coupled to an

output terminal of the buffers for respectively outputting the first, second, third and fourth analog signal.

6. (Original) The driving circuit of claim 5, wherein the plurality of buffers include a first buffer, a second buffer, a third buffer and a fourth buffer, each of the buffers having a first input terminal, a second input terminal and the output terminal; the first input terminal of the each buffer receiving the polarity-inverting signal; the second input terminal of the first buffer receiving the first digital signal; the second input terminal of the second buffer receiving the second digital signal; the second input terminal of the third buffer receiving the third digital signal; the second input terminal of the fourth buffer receiving the fourth digital signal.

7. (Original) The driving circuit of claim 6, wherein the first set of transistors includes a first PMOS transistor and a first NMOS transistor; a gate of the first PMOS transistor and a gate of the first NMOS transistor coupled to the output terminal of the first buffer; a source of the first PMOS transistor coupled to a drain of the first NMOS transistor, a drain of the first PMOS transistor coupled to a power voltage, a source of the NMOS transistor coupled to a ground voltage, the first analog signal outputted through the source of the first PMOS transistor and the drain of the first NMOS transistor.

8. (Original) The driving circuit of claim 7, further comprising three resistors connected in series between the drain of the first PMOS transistor and the source of the first NMOS transistor.

9. (Original) The driving circuit of claim 7, wherein the second set of transistors includes a second PMOS transistor and a second NMOS transistor, a gate of the second PMOS transistor and a gate of the second NMOS transistor coupled to the output terminal of the second buffer, a source of the second PMOS transistor coupled to a drain of the second NMOS transistor, a drain of the first PMOS transistor coupled to the power voltage, a drain of the

second NMOS transistor coupled to the ground voltage, the second analog signal outputted through the source of the second PMOS transistor and the drain of the second NMOS transistor.

10. (Original) The driving circuit of claim 9, further comprising a resistor connected between the drain of the first PMOS transistor and the drain of the second PMOS transistor.

11. (Original) The driving circuit of claim 9, further comprising a resistor connected between the source of the first NMOS transistor and the source of the second NMOS transistor.

12. (Original) The driving circuit of claim 9, wherein the third set of transistors includes a third PMOS transistor and a third NMOS transistor, a gate of the third PMOS transistor and a gate of the third NMOS transistor coupled to the output terminal of the third buffer, a source of the third PMOS transistor coupled to a drain of the third NMOS transistor, a drain of the third PMOS transistor coupled to the power voltage, the source of the third NMOS transistor coupled to the ground voltage, the third analog signal outputted through the source of the third PMOS transistor and the drain of the third NMOS transistor.

13. (Original) The driving circuit of claim 12, further comprising a resistor connected between the drain of the second PMOS transistor and the drain of the third PMOS transistor.

14. (Original) The driving circuit of claim 12, further comprising a resistor connected between the source of the second NMOS transistor and the source of the third NMOS transistor.

15. (Original) The driving circuit of claim 12, wherein the fourth set of transistors includes a fourth PMOS transistor and a fourth NMOS transistor, a gate of the fourth PMOS transistor and a gate of the fourth NMOS transistor coupled to the output terminal of the fourth buffer, a source of the fourth PMOS transistor coupled to a drain of the fourth NMOS transistor, a drain of the fourth PMOS transistor coupled to the power voltage, a source of the fourth NMOS

transistor coupled to the ground voltage, the fourth analog signal outputted through the source of the fourth PMOS transistor and the drain of the fourth NMOS transistor.

16. (Original) The driving circuit of claim 15, further comprising a resistor connected between the drain of the third PMOS transistor and the drain of the fourth PMOS transistor.

17. (Original) The driving circuit of claim 15, further comprising a resistor connected between the source of the third NMOS transistor and the source of the fourth NMOS transistor.

18. (Original) The driving circuit of claim 15, further comprising a resistor connected between the fourth PMOS transistor and the power voltage.

19. (Original) The driving circuit of claim 15, further comprising a resistor connected between the source of the fourth transistor and the ground voltage.